



Sierra Components, Inc.

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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

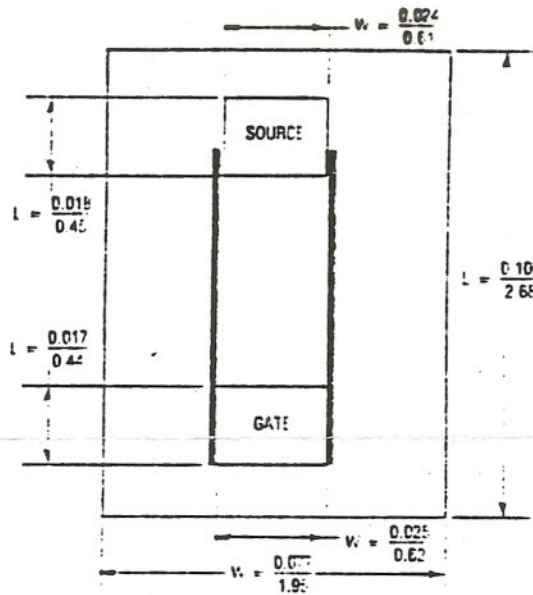


Figure 2. HEX-1: 400V, N-Channel

All dimensions shown in inches/mm
 Die dimensions are from centerline to centerline of scribe alleys

Topside Metal: Al
 Backside: Si
 Backside Potential:
 Mask Ref:
 Bond Pads (Mils): .004"

APPROVED BY: CB
 MFG: IRI

DIE SIZE: .077" x .108"
 THICKNESS: .014"

DATE: 2/8/01
 P/N: IRFC310